REMARKS

Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks.

Amendments

Revisions to the Specification

The Examiner requested correction of certain errors in the specification and Applicant has amended the specification accordingly. No new matter has been added. The amendments are supported in the drawings or elsewhere in the specification.

Amendments to the Claims

As described in the specification, Applicant's invention operates within a unified memory architecture for a computer system. As known in the art, in a unified memory architecture, graphics memory is integrated into main memory and a memory controller controls the use of the main memory between the graphics subsystem and the central processing unit Applicant has amended independent claims 1, 10 and 15 to more particularly point out that Applicant's invention operates in conjunction with such a memory controller. No new matter has been added as a result of these amendments because the specification describes a unified memory architecture that is consistent with the commonly accepted definition in the art. Furthermore, no new issues are raised by these amendments because original independent claim 1 specified that the claimed architecture was a unified memory architecture.

Applicant has also amended dependent claims 2, 11, and 16 to clarify that logical memory address spaces are being mapped into physical memory devices. No new matter has been added as a result of these amendments because the mapping of logical memory address spaces to physical memory devices is described in the specification.

Objections

Objections to the Specification

The Examiner objected to portions of the specification as containing errors that were of a typographical nature. Applicant respectfully requests the withdrawal of the objection in light of the amendments to the specification made herein.

Rejections

Rejections under 35 U.S.C. § 112, first paragraph

Claims 1-3, 6, 9 and 15-19

Claims 1-3, 6, 9 and 15-19 were rejected under the first paragraph of 35 U.S.C. § 112 as unsupported by the specification. Applicant respectfully directs the Examiner's attention to the description of Figure 2 on page 11, lines 5-11, and further to page 18, lines 9-12. Applicant respectfully submits that these sections of the specification support the invention as claimed by Applicant in claims 1-3, 6, 9 and 15-19.

Because the invention operates in a unified memory architecture, the logical address space for graphics memory is part of the total logical address space for main memory. The specification describes an invention that partitions the logical address space within main memory that is assigned to a color buffer into a frame-preparation memory and a refresh memory, i.e., a subset of the addresses within the logical address space of main memory are assigned to each of the frame-preparation and refresh memories. The specification further describes, *intra alia*, 1) an embodiment of the invention in which the logical address spaces within main memory that is assigned to frame-preparation memory and the refresh memory are mapped onto physical devices that make up main memory, as well as 2) an embodiment in which the address space within main memory that is assigned to the refresh memory is mapped onto a physical device that forms a dedicated memory separate from the main memory. Thus, the invention is not restricted to mapping the address space for the frame-preparation memory onto main memory and the address space for the refresh memory onto a dedicated memory as asserted by the Examiner because at least one alternate embodiment is described in the specification. Therefore, Applicant respectfully requests the withdrawal of the rejection of claims 1-3, 6, 9 and 15-19 under 35 U.S.C. § 112, first paragraph.

Rejections under 35 U.S.C. § 112, second paragraph

Claims 2 and 6

Claims 2 and 16 were rejected under 35 U.S.C. § 112, second paragraph because the Examiner interpreted them as contradicting their parent claims. Applicant respectfully disagrees with the rejection because the clarity of claim language must be analyzed in light of the teachings of the prior art and the specification as it would be interpreted by

one of skill in the art [MPEP 2173.02]. Applicant respectfully submits that one of ordinary skill in the data processing arts would understand from the specification that claims 2 and 16 are directed to an embodiment of the invention that is a subset of the invention claimed in independent claims 1 and 15, and thus claims 2 and 16 do not contradict claims 1 and 15. Additionally, Applicant has amended claims 2 and 16 to further clarify their claimed subject matter. Therefore, Applicant respectfully requests the withdrawal of the rejection of claim 2 and 16 under 35 U.S.C. § 112, second paragraph.

Rejections under 35 U.S.C. § 103

Claims 1-3, 5, 10-12, 15-16 and 18

Claims 1-3, 5, 10-12, 15-16 and 18 were rejected under 35 U.S.C. § 103(a) as being obvious over Stortz (U.S. Patent 5,900,855) in view of Asaro et al. (U.S. Patent 6,100,906). Applicant notes that Asaro qualifies as prior art only under § 102(e) and reserves the right to swear behind the reference at a later date. Nonetheless, Applicant respectfully submits that the invention as claimed in claims 1-3, 5, 10-12, 15-16 and 18 is patentable over the combination of Stortz and Asaro because the combination does not teach or suggest each and every element of the invention as claimed.

Stortz discloses a video controller that controls video memory on a graphics card. The video control also uses a portion of system memory as an incremental video buffer when there is insufficient video memory on the graphics card to process a video frame. To avoid contention between the system memory controller and the video controller for the same memory space, the portion of system memory representing the incremental video buffer is deallocated from the system memory controller.

Asaro discloses a video graphics circuit containing a video processing module that manages two buffers in video memory. A central processor reads data blocks from a system memory and sends the data blocks to the video graphics circuit for processing and displaying.

Both Stortz and Asaro disclose graphics subsystems containing a video processor/controller for controlling memory within the graphics subsystem that is dedicated to video processing. The video processors/controllers in Stortz and Asaro are both separate from the processor/controller that manages the memory of the system used by the central processing unit. Thus, by definition, neither Stortz nor Asaro teach or

suggest a unified memory architecture as specified by Applicant in amended independent claims 1, 10 and 15. Furthermore, the video processors/controllers in the graphics subsystems of Stortz and Asaro do not manage the use of main/system memory between a graphics subsystem and another processing unit as claimed by Applicant in amended independent claims 1, 10 and 15. In particular, neither Stortz nor Asaro teach or suggest a memory controller that partitions an address space for a color buffer within main memory into two logical buffers. Therefore, because neither Stortz or Asaro teach or suggest each and every limitation of Applicant's invention as claimed in independent 1, 10 and 15, and the claims that depend from them, the combination cannot be properly interpreted as doing do. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claims 1-3, 5, 10-12, 15-16 and 18 under 35 U.S.C. § 103(a) over the combination of Stortz and Asaro.

Claims 4, 13 and 17

Claims 4, 13 and 17 were rejected under 35 U.S.C. § 103(a) as being obvious over Stortz in view of Asaro and further in view of Swan (U.S. Patent 6,304,297 B1). Applicant notes that Swan qualifies as prior art only under § 102(e) and reserves the right to swear behind the reference at a later date. Nonetheless, Applicant respectfully submits that the invention as claimed in claims 4, 13 and 17 is patentable over the combination of Stortz, Asaro and Swan because the combination does not teach or suggest each and every element of the invention as claimed.

Claims 4, 13 and 17 depend from amended independent claims 1, 10 and 15. Because the combination of Stortz and Asaro does not teach or suggest each and every element of claims 1, 10 and 15, Swan must fill the gaps in order to have a proper *prima facie* case of obviousness.

Swan discloses a video process that adjusts video rates by adding or deleting frames using a frame buffer and a memory. Swan neither teaches nor suggests that the video processor manages the use of main memory between a graphics subsystem and a processing unit as claimed by Applicant in amended independent claims 1, 10 and 15 from which claims 4, 13 and 17 depend. Therefore, the combination of Stortz, Asaro and Swan does not teach or suggest each and every limitation of claims 4, 13 and 17, and

Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

Claims 6-9, 14, 19, 20-21

Claims 6-9, 14, 19, 20-21 were rejected under 35 U.S.C. § 103(a) as being obvious over Stortz in view of Asaro and further in view of Naughton et al. (U.S. Patent 5,519,825). Applicant respectfully submits that the invention as claimed in claims 6-9, 14, 19, 20-21 is patentable over the combination of Stortz, Asaro and Naughton because the combination does not teach or suggest each and every element of the invention as claimed.

Claims 6-9, 14, 19, 20-21 depend from amended independent claims 1, 10 and 15. Because the combination of Stortz and Asaro does not teach or suggest each and every element of claims 1, 10 and 15, Naughton must fill the gaps in order to have a proper *prima facie* case of obviousness.

Naughton discloses a video cache buffer that stores a subset of data used to create a video frame for display. In one embodiment, the central processing unit allocates a portion of main memory to serve as the video cache buffer. The central processing unit also allocates portions of video RAM as front and back frame buffers. Thus, Naughton does not teach or disclose a memory controller that partitions an address space in main memory that is assigned to a color buffer into two logical buffers as claimed by Applicant in amended independent claims 1, 10 and 15 from which claims 6-9, 14, 19, 20-21 depend. Therefore, the combination of Stortz, Asaro and Naughton does not teach each and every limitation of claims 6-9, 14, 19, 20-21, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

New Claims

Applicant has added new claims 22-26 to claim the subject matter of the originally claims in means-plus-function form. The new claims are allowable for at least the reasons given above for claims 1-21.

SUMMARY

In this response, claims 1, 2, 10, 11, 15, 16 and 21 have been amended, and new claims 22-26 have been added, with no claims cancelled. Therefore, claims 1-26 are currently pending. In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Sue Holloway at (408) 720-3476.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR
& ZAFMAN LLP

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Sheryl S. Holloway
Attorney for Applicant
Registration No. 37,850

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-3476

VERSION OF AMENDMENTS WITH MARKINGS

In the Specification

Please replace the paragraph starting at line 20, page 8 with the following:

It will be appreciated that the computer system 1 is one example of many possible computer systems which have different architectures. The computer system of FIG. 1 may be, for example, an Apple Macintosh computer, such as an Apple iMac computer. FIG. 1 is also illustrative of personal computers based on an Intel microprocessor. Such personal computers often have multiple buses, one of which can be considered to be a peripheral bus. Network computers are another type of computer system that can be used with the present invention. Network computers do not usually include a hard disk or other mass storage, and the executable programs are loaded from a network connection into the RAM 12 for execution by the microprocessor 10. A Web TV system, which is known in the art, is also considered to be a computer system according to the present invention, but it may lack some of the features shown in FIG. 1, such as certain input or output devices. A typical computer system will usually include at least a processor, memory, and a bus connecting the memory to the processor.

Please replace the paragraph starting at line 5 on page 11 with the following:

As is conventional, the address space of the video memory is logically divided into several types of buffers, including a frame buffer which is further subdivided into buffers that handle various attributes of a frame, such as color buffer 204. In the present invention, the memory controller 20[7]1 logically partitions the address space of the color buffer 204 into a frame-preparation memory 205 and a refresh memory 207. The address space of the frame-preparation memory 205 is mapped to the main memory 203, while the address space of the refresh memory 207 is mapped to a separate, dedicated memory.

Please replace the paragraph starting at line 3 on page 12 with the following:

Partitioning the memory address space of the color buffer into the frame-preparation memory 205 and the refresh memory 207 decouples the color buffer from main memory by directing the memory traffic necessary to refresh the display device 219 to the separate, dedicated memory instead of to the main memory. The only color data directed to the main memory 203 is for the purpose of forming of a new frame in frame-preparation memory 205 and the extra bandwidth previously required to refresh the display device 219 is now off-loaded to the separate refresh memory 207. This can be an i[I]mportant change since the bandwidth for refresh rate is actually less than the bandwidth for frame formation. Thus, the overall bandwidth requirement of the main memory 203 for graphics operations [are] is reduced by the amount of bandwidth required to sustain the refresh rate of the display device 219.

IN THE CLAIMS

1. (Amended) A unified memory architecture that decouples a color buffer from a main memory in a computer, the architecture comprising:

a memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and a processing unit, the memory controller operable for partitioning an address space for the color buffer in main memory into two logical buffers, operable for designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory, operable for connecting the frame-preparation memory to [a] the graphics subsystem and operable for connecting the refresh memory to a display device, wherein color data is written into the frame-preparation memory at a frame rate and read from the refresh memory at a rate that supports a refresh rate of the display device.

2. (Amended) The unified memory architecture of claim 1, wherein the address space for the refresh memory is mapped into a physical memory device for a dedicated memory that is separate from a physical memory device for the main memory.

10. (Amended) A method of decoupling a color buffer from a main memory by a memory controller in a computer having a unified memory architecture, the memory controller managing use of the main memory between a graphics subsystem and a processing unit, the method comprising:

partitioning an address space for the color buffer in the main memory into first and second logical buffers;

designating the first logical buffer as a refresh memory and designating the second logical buffer as a frame-preparation memory;

writing color data into the frame-preparation memory at a frame rate;

copying the color data from the frame-preparation memory to the refresh memory; and

reading the color data from the refresh memory at a rate that supports a refresh rate of a display device.

11. (Amended) The method of claim 10, further comprising:

mapping the address space for the refresh memory onto a physical memory device for a dedicated memory separate from a physical memory device for the main memory.

15. (Amended) A computer system having a unified memory architecture, the computer system comprising:

a processing unit;

a main memory connected to the processing unit though a system bus, the main memory being partitioned into an address space for a color buffer;

a memory controller connected to the main memory to manage use of the main memory between a graphics subsystem and the processing unit;

a graphics subsystem connected to the main memory through the memory controller to create a frame of color data in the color buffer at a frame rate; and

a display device connected to the main memory through the memory controller, to display a frame of color data from the color buffer at a refresh rate,

wherein the memory controller decouples the color buffer from the main memory by:

partitioning the address space for the color buffer in main memory into two logical buffers;

[for] designating one logical buffer as a frame-preparation memory and one logical buffer as a refresh memory;

connecting the frame-preparation memory to the graphics subsystem;

connecting the refresh memory to the display device; and

copying the color data from the frame-preparation memory to the refresh memory.

16. (Amended) The computer system of claim 15, further comprising a memory device for a dedicated memory separate from a memory device for the main memory and the memory controller further maps the address space for the refresh memory to the memory device for the dedicated memory.

21. (Amended) The [unified memory architecture] computer system of claim [7]20, wherein the memory controller switches the designations of the logical buffers when an entire frame of color data is ready for display in the logical buffer currently designated as the frame-preparation memory.